**LOW POWER 4T SRAM CACHE**

A PROJECT REPORT

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**ABSTRACT**

Memory refers to the physical devices used to store program or data on a temporary or permanent basis for use in a [computer](http://en.wikipedia.org/wiki/Computer) or other [digital](http://en.wikipedia.org/wiki/Digital) [electronic](http://en.wikipedia.org/wiki/Electronics) device. Semiconductor memory is an electronic [data storage device](http://en.wikipedia.org/wiki/Data_storage_device), often used as [computer memory](http://en.wikipedia.org/wiki/Computer_memory), implemented on a [semiconductor](http://en.wikipedia.org/wiki/Semiconductor)-based [integrated circuit](http://en.wikipedia.org/wiki/Integrated_circuit). It forms an integral part of many computer and data processing integrated circuits. On chip caches can effectively reduce the speed gap between the processor and main memory. Almost all microprocessors employ them to boost system performance.

The cost and performance of an embedded system heavily depends on the kind of memory devices it utilizes. Due to high demands on portable products power consumption is a major concern in VLSI chip and microprocessor designs. Low power consumption is highly desirable in battery powered embedded systems. Such systems generally employ memory devices which can operate at low and ultra-low voltage levels. Hence embedded caches need to operate at a faster rate and also consume less power.

Conventionally, cache memories are implemented using 6T SRAM cells. This project aims to implement cache memory using 4T SRAM cells which consume less area compared to that of 6T SRAM cells. Access time of 4T SRAM cache is greater than that of 6T SRAM cache. The performance of 4T cache is improved by implementing divided bitline technique to reduce delay and power consumption.

Further, Microwind tool is used for creating layouts of both 6T and 4T cache memories of size 8x16. Simulation results are compared for both cases in terms of area, power and access delay. Divided bitline technique is applied on a column of 128 cells and from the simulation results it is shown that access delay is reduced.

**LIST OF FIGURES**

**LIST OF TABLES**

**LIST OF ABBREVIATIONS**

**TABLE OF CONTENTS**

ACKNOWLEDGEMENT i

ABSTRACT ii

LIST OF FIGURES iii

LIST OF TABLES iv

LIST OF ABBREVIATIONS v

**CHAPTER 1 INTRODUCTION**

**CHAPTER 1**

**INTRODUCTION**

**1.1 MOTIVATION**

Power reduction in SoC based embedded systems, is one of the important design specifications of VLSI design. This project deals with the reduction in delay and power consumed by memory in SoC with acceptable trade off of stability and performance.

SoCs integrate multiple functions on a single silicon die. As process geometries have scaled, designs which use more and more of the additional silicon real estate available on chips to integrate embedded memories evolved. These embedded memories allow for significantly better system performance and lower power compared to a solution where off-chip memories are used. Most current designs have over 50% of their area used by embedded memories and these memories account for 50-70% of the total SoC power dissipation. Clearly, any attempt to reduce SoC power is incomplete if it does not attempt to reduce the power consumed by the embedded memories in the design.

Embedded cache memories are implemented using SRAM cells. SRAM is a type of [semiconductor](http://en.wikipedia.org/wiki/Semiconductor) memory that uses [bi-stable](http://en.wikipedia.org/wiki/Multivibrator) [latching circuitry](http://en.wikipedia.org/wiki/Flip-flop_(electronics)) to store each bit. A conventional SRAM has a 6T design. It is volatile in the conventional sense that data is eventually lost when the memory is not powered. So designing the SRAMs which consume less power becomes crucial. The cache is a smaller, faster memory which stores copies of the data from the most frequently used [main memory](http://en.wikipedia.org/wiki/Main_memory) locations. As long as most memory accesses are cached memory locations, the accesses time of memory will be closer to the accesses time of cache than to the access time of main memory. Hence improving the speed of cache becomes important.

**1.2 OBJECTIVE**

The objective of this project is to implement a cache memory using 4T SRAM and compare it with conventional 6T SRAM cache for parameters like power, area and speed of operation, then implement buffered bit-line technique on 4T SRAM cache to get an optimized design with low power and lesser delay.

**CHAPTER 2**

**LITERATURE SURVEY**

**2.1 INTRODUCTION**

**2.2 PAPER 1**

**Title:**Arash Azizi Mazreah, Mohammad Noorollahi Romani, Mohammad Taghi Manzuri, Ali Mehrparvar, *“A low power and high density cache memory on novel SRAM cell”*, IEICE Electronics Express, Vol.6, August 2009

**2.2.1 OBJECTIVE**

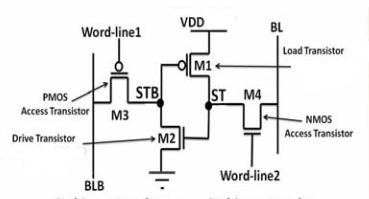
The objective is to develop an SRAM cell with four transistors to reduce the cell area size and power consumption with no performance degradation.

**2.2.2 INTRODUCTION**

Conventional SRAMs that use 6T SRAM cells have difficulty in meeting the growing demand for a larger memory capacity in mobile applications. Furthermore, in a conventional SRAM cell one of the two bit-lines must be discharged regardless of the written value. Therefore the power consumption in writing both “0” and “1” are the same. Also during the read operation one of the two bit-lines must be discharged irrespective of the value stored in the cell. Therefore there are always transitions on bit-lines in both writing “0” and “1” and reading “0” and “1”. Furthermore 6T SRAM cell uses full swing on wordlines and these cause high dynamic power consumption during read and write operations. In response to this requirement an SRAM with 4 transistors is developed. The power consumption of writing and reading zeros in novel cell is much smaller than ones, thus the average power consumption is reduced in caches based on this novel cell.

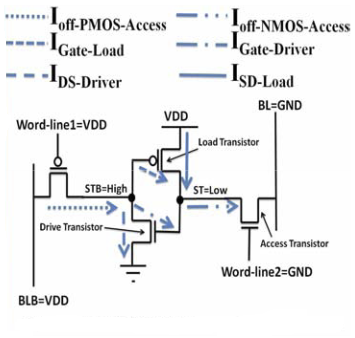
**2.2.3 CELL DESIGN CONCEPT**

Fig (2.1) shows the circuit equivalent to the developed 4T SRAM cell.

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**Fig (2.1) 4T SRAM Cell**

When “1” is stored in the cell, load and drive transistors are ON and there is a positive feedback between ST and STB node. Therefore STB node is pulled to GND by drive transistor and ST node is pulled to VDD by load transistor.

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**Fig (2.2) 4T SRAM Cell in idle mode when “0” is stored**

When “0” is stored in the cell both load and drive transistors are OFF and for data retention without refresh cycle, the following conditions must be satisfied.

IOff-NMOS-access > ISD-Load + IGate-Driver + IGate-Load **Eq (2.1)**

IOff-PMOS-access > IDS-Load + IGate-Driver + IGate-Load **Eq (2.2)**

Fig (2.2) shows leakage current of cell during idle mode for data retention when “0” is stored in the cell. For satisfying the above condition when “0” is stored in the cell we use leakage current of access transistors, especially sub-threshold current of access transistors (IOff-NMOS-access and IOff-PMOS-access ).

To achieve this we can use high threshold voltage for load and drive transistors to reduce sub-threshold currents of these transistors. Low threshold voltage can be used for access transistors; hence leakage current of access transistors will be greater than leakage currents of load and drive transistors. With this threshold voltage assignments above conditions can be satisfied and “0” can be stored in a cell successfully. Leakage currents also depend on the width of the transistors. As width of a transistor increases, leakage currents also increase. As the leakage currents of access transistors should be greater than leakage currents of load and drive transistors, the width of access transistors should be greater than the width of load and drive transistors.

The specifications for 4T SRAM cell are mentioned as follows:

Technology used: 65nm

VDD = 1.2V

(W/L)M1=130nm/65nm­ (W/L)M2 = 130nm/65nm­

(W/L)M3=260nm/65nm­ (W/L)M4 = 260nm/65nm­

Normal threshold voltage: VTN = 0.32V VTP = 0.33V

High threshold voltage: VTN = 0.52V VTP = 0.53V

**2.2.4 WRITE AND READ OPERATION**

* **Write operation:** When a write operation is issued the memory cell will go through the following steps.

**1) Bit-line driving:** For a write, data is placed on BL and its compliment is placed on BLB, then WL1 and WL2 are asserted to GND and VDD respectively.

**2) Cell flipping:** This step includes two states as follows.

**(a) When data is logic ‘0’:** In this state, ST node is pulled down to GND by NMOS access transistor STB node will be pulled up to VDD by PMOS access transistor.

**b) When data is logic ‘1’:** In this state, ST node pulled up to VDD-VTN by NMOS access transistor, and therefore the drive transistor will be ON and STB node will be pulled up to VTP by PMOS access transistor. Load and drive transistors will be ON and positive feedback is created by load and drive transistors between ST and STB nodes.

**3) Idle mode:** At the end of write operation, cell will go to idle mode and WL1 and WL2 are asserted to VDD and GND respectively and BL and BLB return to GND and VDD respectively.

* **Read operation:**

When a read operation is issued the memory cell will go through the following steps.

**1) Bit-line Pre-charging:** For a read, BLB is pre-charged to VDD and then floated. Since, in idle mode BLB maintained at VDD, this step doesn’t include any dynamic energy consumption.

**2) Word-line activation:** In this step WL1 is asserted to GND and two states can be considered.

**(a) Stored data is “1”:** When voltage of STB node is low, the voltage of BLB pulled up to low voltage by NMOS access transistor. We refer to this voltage of BLB as VBLB-LOW.

**(b) Stored data is “0”:** When voltage of STB node is high, the voltage of BLB and STB node are equalized. Since in this state, there is very small different between BLB and STB node, power consumption is very small.

**3) Sensing:** After WL1 is deactivated, the sense amplifier is enabled to read data on BLB.

**4) Idle mode:** At the end of read operation, cell will go to idle mode and BLB is asserted to VDD.

**2.2.5 LEAKAGE CURRENTS**

4T SRAM cell has to retain its value using leakage currents in one state (when “0” is stored) whereas in another state it retains the data using positive feedback (when “1” is stored). In idle mode when “1” is stored, load and drive transistors are ON thereby creating a positive feedback leakage and access transistors have sub-threshold current. But since load and drive transistors have high threshold voltage, therefore there are paths from supply to ground. Thus leakage current in “1’’ state is greater than that in “0’’ state.Leakage current of 6T SRAM cell when ‘‘0’’ or ‘‘1’’ stored is approximately equal to leakage current of 4T SRAM cell when ‘‘1’’ is stored.Leakage current of 4T SRAM cell when ‘‘0’’ is stored is much smaller than leakage current of 6T SRAM cell when ‘‘0’’ or “1” is stored. Most bits of caches are zeros for both data and instruction streams, so average leakage current is smaller in case of 4T SRAM cache when compared to 6T SRAM cache.

**2.2.6 EXPERIMENTAL RESULTS**

**Dynamic power consumption:**

In idle mode BL and BLB are maintained at GND and VDD, hence there is no transition on bit-lines while writing ‘0’.Hence in 4T SRAM power consumed for writing ‘‘0’’ is smaller than that needed for writing ‘‘1’’, whereas in 6T SRAM both cases consume same power. Further in 4T SRAM cell, when “0” is read from cell, there is no transition on BLB and hence power consumption of reading ‘0’ is smaller than reading “1”. In 6T power consumed for reading and writing “1” is same.

From H-SPICE simulations it is obtained that:

* Power consumption of writing “1” in 4T cell is approximately equal with power consumption of writing “1” or “0” in 6T cell.
* Power consumption of reading “1” or “0” in 4T cell are smaller than power consumption of reading “1” or “0” in 6T cell.
* Average dynamic power consumption of new cell is 40% smaller than that of 6T cell.
* Static power consumption of new cell is 20% less than that of 6T cell.

**Cell area:** The new cell size is 20% smaller than conventional 6T cell size.

**2.2.7 CONCLUSION**

* **Advantages:** Cell area, static power consumption and dynamic power consumption have decreased.
* **Disadvantages:** Delay has increased and SNM has decreased.

**2.3 PAPER 2**

**Title:**

Stefan Cosemans, Wim Dehaene and Francky Catthoor, *“A Low-Power Embedded SRAM for Wireless Applications”*, IEEE Journal of Solid- State circuits, Vol. 42, No. 7, July2007

**2.3.1 OBJECTIVE**

The objective of this paper is to introduce a novel ultra-low-power SRAM in which large power reduction is obtained by the use of four new techniques that allow for a wider and better trade-off between area, delay and active and passive energy consumption.

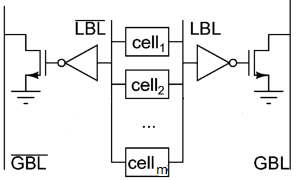
**2.3.2 INTRODUCTION**

Embedded memories play a crucial role in contemporary electronic systems. They are used in different sizes ranging from a few kilobytes for local scratchpads to a few megabytes for on-chip caches. This paper focuses on embedded SRAMs smaller than 1 Mb for use in the lowest levels of the memory hierarchy. Memories at this level of the hierarchy are used very intensively, so their energy consumption has a signiﬁcant impact on the energy consumption of the entire system. In this paper, a novel SRAM design is introduced. The implemented design techniques consist of a more efﬁcient memory databus, the exploitation of the dynamic read stability of SRAM cells, a new low-swing write technique and a distributed decoder.

**2.3.3 SHORT BUFFERED BITLINE TECHNIQUE**

In traditional low-power memory designs, the cell read current Iread,cell must create a large enough voltage difference onthe bit-lines. Since the bit-line capacitance is very large, this stepmakes up a large part of the memory access delay. Therefore Iread,cell must be made as large as possible, which results in high cell leakage currents because a large requires large transistor widths, low threshold voltages or a high supply voltage for the cell. Nominal value of Iread,cell is important. Because the cells need to be very small, the intra-die variation of Iread,cell will be large. This requires a large safety margin on the memory delay. Since all cells will remain activated until the slowest cell is ready, this also causes an important increase in energy consumption.

These problems are remedied when the amount of charge that the cell must draw from the bit-line is reduced. Therefore, the bit-line is divided into shorter local bit-lines. Buffer connects local and global bit-lines as shown in fig (2.3). Inverter acts as a sensing element for the buffer. LBL uses a large voltage swing but since capacitance is less, it has limited impact on energy consumption. Buffer consists of a scaled up NMOS transistor. Iread,buffer can be much larger than Iread,cell and suffers less from intra-die variation. Low voltage power supply can be used as precharge voltage to the GBL which reduces power consumption.



**Fig (2.3) Buffered Bit-lines**

**Impact on Memory Databus:**

In traditional designs, amplification at the column level is required to limit Iread,cell impact on memory speed. In buffered bit-line approach, buffer can easily deliver more current so global bit-lines can be directly extended to memory output. Only one set of sense amplifiers is required for entire memory so area overhead is reduced.

|  |  |
| --- | --- |
| **Traditional Solution** | **Proposed Solution** |
| C:\Users\nikhila\Desktop\Capture2.PNG | C:\Users\nikhila\Desktop\Capture3.PNG |

**Fig (2.4) Memory databus**

**2.3.4 CONCLUSION**

* **Advantages:** Since short bit-lines are used, capacitance offered has decreased. Hence power and delay have reduced.
* **Disadvantages:** Instead of using a single bit-line, number of LBLs and a GBL are being used, due to whicharea overhead has increased.
  1. **PAPER 3**

**Title:**

Karandikar and K. K. Parhi, *“Low power SRAM design using hierarchical divided bit-line approach,”* in Proc. Int. Conf. Computer Design: VLSI in Computers and Processors, 1998, pp. 82–88.

**2.4.1 OBJECTIVE**

This objective of this paper is to present a novel hierarchical divided bit-line approach for reducing active power in SRAMs by reducing bit-line capacitance.

**2.4.2 INTRODUCTION**

Designing a low power system not only reduces weight and size of batteries for portable systems but also helps in reducing the ever important packaging costs of integrated circuits. To this end, the design of low power digital systems is becoming increasingly important. This paper describes a novel divided bit-line approach for reducing the active power by reducing the bit-line capacitance and then extends it to a hierarchical divided bit-line approach. It is shown that by reducing this capacitance, not only power reduction is achieved but also access time is reduced. Two or more 6T SRAM cells are combined together to divide the bit-line in to several sub bit- lines. These sub bit-lines are again combined to form two or more levels of hierarchy. Optimum values for number of levels of hierarchy and number of blocks combined at each level have been derived.

**2.4.3 CONCEPT**

**2.4.4 EXPERIMENTAL RESULTS**

A 2K x 8 bits SRAM chip using MAGIC layout tool is designed; 6 and 8 cells are combined at the sub bit-line level.

* Active power consumption has reduced approximately by 50-60%.
* Access time is reduced by 30%.

**2.4.5 CONCLUSION**

* **Advantages:** By dividing bit-line into sub bit-lines, SRAM cells become more stable, as they are guarded from the noise on bit-lines through pass transistors. Active power consumption and access time have decreased.
* **Disadvantages:** Due to hierarchical bit-line setup area overhead increases.

**CHAPTER 3**

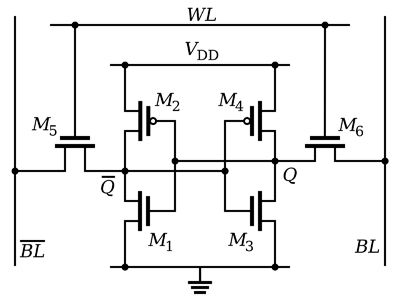
**SRAM CONCEPTS**

**3.1 INTRODUCTION**

The memory circuit is said to be static if the stored data can be retained indefinitely as long as a sufficient power supply voltage is provided, without any need for a periodic refresh operation. SRAMs have three operational modes. When the cell is in “hold” state the value of the bit is stored in the cell for future usage. During a “write” operation, logic ‘0’ or ‘1’ is fed to the cell for storage. The value of the stored bit is transmitted to the outside world during a “read” operation. In this chapter the concepts of 6T and 4T SRAM cells are discussed. Different operations (read, write and hold) taking place and the working in detail are explained for both types of SRAM cells.

**3.2 6T SRAM CELL**

6T SRAM cell shown in Fig (3.1) uses a simple bistable latch circuit to hold a data bit. A pair of cross coupled inverters provides the storage while two access transistors (NFETs) provide read and write operations. The access transistors are controlled by the word line signal WL that defines the operational modes.



**Fig (3.1) 6T SRAM Cell**

**3.2.1 WORKING**

The cell works in three operating modes.

**Hold state:** When WL=0, both access FETs are OFF and the cell is isolated. This defines the “hold’’ condition and the cell retains the value stored. Both bit and bit-bar lines are precharged to VDD during this state.

**Write operation:**

To perform ‘‘write’’ operation, the word line is brought up to a value of WL=1. This turns ON the access transistors and bit, bit-bar lines get connected to the write circuitry. Value to be written is placed on bit line and its complimentary value is placed on bit-bar line. Precharge remains off during write operation.

When logic ‘1’ is written into the cell, bit line is made high and bitbar line is made low. Referring to the fig (2.1), access transistors M5 and M6 are turned ON. Node Q is charged to VDD which turns M1 ON and M2 OFF. M1 pulls Q**—** node to ground. M3 turns OFF and M4 is turned ON which pulls node Q to VDD.

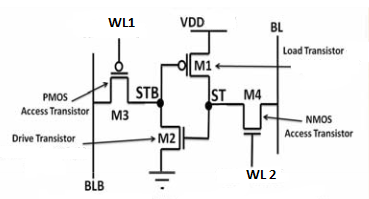
When logic ‘0’ is written into the cell, bit line is made low and bitbar line is made high. Referring to the fig (2.1), access transistors M5 and M6 are turned ON. Node Q is pulled down to logic ‘0’ value which turns M2 ON and M1 OFF. M2 pulls Q**—** node to VDD. M4 turns OFF and M3 is turned ON which pulls node Q to ground.

**Read operation:** During the read operation wordline is made high, WL=1. This turns on the access transistors and bit, bit-bar lines get connected to read circuitry. Precharge remains OFF during read operation. Bit and bitbar lines act as outputs and are fed into a sense amplifier that determines the stored state.

**3.3 4T SRAM CELL**

4T SRAM cell consists of load and driver transistors and two access transistors. Unlike in 6T cell where both the access transistors are NFETs, in 4T cell one of the access transistors is a PFET.

Two different word lines WL1 and WL2 are used for controlling PFET and NFET access transistors respectively.



**Fig (3.2) 4T SRAM Cell**

**2.3.1 WORKING**

The cell works in three operating modes.

* **Hold state:** When WL1= ‘1’ and WL2= ‘0’, both access transistors are OFF and the cell is isolated. This defines the “hold’’ condition and the cell retains the value stored. Different precharge voltages are used for bit and bitbar lines. Bit line is precharged to VDD and bitbar line is precharged to ground during this state.
* **Write operation:**

When a write operation is issued the memory cell will go through the following steps.

**1) Bit-line driving:** For a write, data is placed on BL, and then WL2 asserted to VDD, but voltages on word-line1 and BLB maintained at idle mode ( WL1= VDD and VBLB =VDD). Only precharge on bitline is turned OFF.

**2) Cell flipping:** This step includes two states as follows.

**(a) When data is logic ‘0’:** In this state, ST node is pulled down to GND by NMOS access transistor, and therefore the drive transistor will be OFF. STB node will be floated and then pulled up to voltage of BLB (VDD) by leakage current of PMOS access transistor and thus load transistor will be OFF.

**b) When data is logic ‘1’:** In this state, ST node pulled up to VDD-Vtn by NMOS access transistor, and therefore the drive transistor will be ON , and STB node will be pulled down to GND, thus load transistor will be ON which further pulls up ST node to VDD.

**3) Idle mode:** At the end of write operation, cell will go to idle mode and WL2 and BL are asserted to GND.

* **Read operation:**

When a read operation is issued the memory cell will go through the following steps.

**1) Bit-line Pre-charging:** For a read, BL pre-charged to GND and then floated. Since, in idle mode BL maintained at GND, this step doesn’t include any dynamic energy consumption.

**2) Word-line activation:** In this step WL2 asserted to VDD and two states can be considered.

**(a) Voltage of ST node is high:** When voltage of ST node is high, the voltage of BL pulled up to high voltage by NMOS access transistor. We refer to this voltage of BL as VBL-HIGH.

**(b) Voltage of ST node is low:** When voltage of ST node is low, the voltage of BL and ST node equalized. Since in this state, there is very small different between BL and ST node, power consumption is very small.

**3) Sensing:** After WL2 is deactivated, the sense amplifier is enabled to read data on BL.

**4) Idle mode:** At the end of read operation, cell will go to idle mode and WL2 and BL are asserted to GND respectively.

**CHAPTER 4**

**DESIGN CONSIDERATIONS**

**4.1 INTRODUCTION**

To determine the (W/L) ratios of the transistors in a SRAM cell a number of design criteria must be taken into consideration. In this chapter the design criteria for 4T and 6T SRAM cells are mentioned and conditions for transistor sizes are determined for proper read and write operations to occur.

**4.2 DESIGN CONSIDERATIONS OF 6T SRAM CELL**

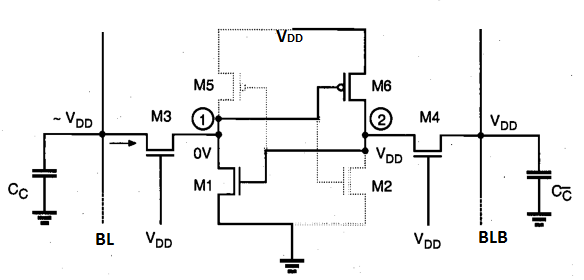
The two basic requirements which dictate the (W/L) ratios in a typical CMOS SRAM cell are:

(a) The data-read operation should not destroy the stored information in the SRAM cell.

(b) The cell should allow modification of the stored information during the data-write phase.

**Read “0" operation:**

Consider the data read operation first, assuming that logic "0" is stored in the cell. The voltage levels in the CMOS SRAM cell at the beginning of the "read" operation are depicted in Fig (4.1). Here, the transistors M2 and M5 are turned OFF, while the transistors M1 and M6 operate in the linear the linear mode. Thus, the internal node voltages are V1=0 and V2=VDD before the cell access (or pass) transistors M3 and M4 are turned on. The active transistors at the beginning of the data-read operation are highlighted in Fig (4.1).



**Fig (4.1) Voltage levels in the SRAM cell at the beginning of the read “0” operation**

After the pass transistors M3 and M4 are turned on by the row selection circuitry, the voltage level of column C will not show any significant variation since no current will flow through M4. On the other half of the cell, however, M3and Ml will conduct a nonzero current and the voltage level of column C will begin to drop slightly. Note that the column capacitance Cc is typically very large; therefore, the amount of decrease in the column voltage is limited to a few hundred millivolts during the read phase. The data- read circuitry is responsible for detecting this small voltage drop and amplifying it as a stored "0" While MI and M3 are slowly discharging the column capacitance, the node voltage V1, will increase from its initial value of 0 V. Especially if the (W/L) ratio of the access transistor M3 is large compared to the (W/L)ratio of M1, the node voltage V1 may exceed the threshold voltage of M2 during this process, forcing an unintended change of the stored state.

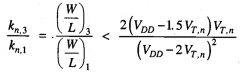
The key design issue for the data-read operation is then to guarantee that the voltage V1, does not exceed the threshold voltage of M2, so that the transistor M2 remains turned off during the read phase, i.e.

C:\Users\nikhila\Desktop\6tr1.PNG Eq (4.1)

We can assume that after the access transistors are turned ON the column voltage Vc remains approximately equal to VDD. Hence, M3 operates in saturation while M1 operates in the linear region.

C:\Users\nikhila\Desktop\eqre2.PNG Eq (4.2)

Combining this equation with Eq (4.1) results in:

 Eq (4.3)

The upper limit of the aspect ratio found above is actually more conservative, since a portion of the drain current of M3 will also be used to charge-up the parasitic node capacitance of node1.

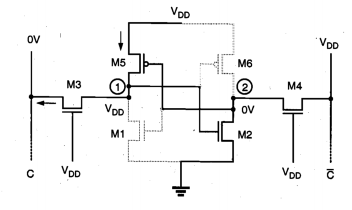
To summarize, the transistor M2 will remain in cut-off during the read "0" operation if Eq (4.3) is satisfied. A symmetrical condition also dictates the aspect ratios of M2 and M4.

Now substituting VDD = 0.5V and VT,n = 0.2V ; standard values in 50nm technology in “Microwind”, we get Eq (4.3) as W3 ≤ 8(W1) and similarly we obtain W4 ≤ 8( W2). From the layout W1 = W2 = 9 lambda, hence we obtain

W3 ≤ 72 lambda and W4 ≤ 72 lambda.

**Write “0” when “1” is stored:**

Now consider the write "0” operation, assuming that a logic "1" is stored in the SRAM cell initially. Fig (4.2) shows the voltage levels in the CMOS SRAM cell at the beginning of the data-write operation. The transistors M1 and M6 are turned OFF, while the transistors M2 and M5 operate in the linear mode. Thus, the internal node voltages are V1 = VDD and V2 = 0 V before the cell access (or pass) transistors M3 and M4 are turned ON.

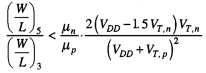


**Fig (4.2) Voltage levels in the SRAM cell at the beginning of the "write" operation.**

The column voltage VC is forced to logic "0" level by the data-write circuitry; thus, we may assume that Vc is approximately equal to 0 V. Once the pass transistors M3 and M4 are turned ON by the row selection circuitry, we expect that the node voltage V2 remains below the threshold voltage of Ml, since M2 and M4 are designed according to Eq (4.3). Consequently, the voltage level at node (2) would not be sufficient to turn ON Ml. To change the stored information, i.e., to force V1 to 0 V and V2 to VDD, the node voltage V1 must be reduced below the threshold voltage of M2, so that M2 turns OFF first. When V1 = VTn the transistor M3 operates in the linear region while M5 operates in saturation.

C:\Users\nikhila\Desktop\eq wr1.PNG Eq (4.4)

C:\Users\nikhila\Desktop\eqwr2.PNG Eq (4.5)

Eq (4.6)

To summarize, the transistor M2 will be forced into cut-off mode during the write "0" operation if Eq (4.6) is satisfied. This will guarantee that Ml subsequently turns ON, changing the stored information. Note that a symmetrical condition also dictates the aspect ratios of M6 and M4.

Now substituting VDD = 0.5V and VT,n = 0.2V ; standard values in 50nm technology in “Microwind” and taking µn/ µp = 2.5 we get Eq (4.6) as

W3 > 2.45 (W5) and similarly we obtain W4 > 2.45 (W6).

From the layout W5 = W6 = 5 lambda, hence we obtain W3 > 12.25 lambda and W4 > 12.25 lambda.

**4.3 DESIGN COSIDERATIONS OF 4T SRAM CELL**